April 24th 2015

Half Day Tutorial:

The Memories of Tomorrow: Technology, Design, Test, and Dependability

Presenter: Elena Ioana VATAJELU

In the framework of the IEEE DTIS 2015 conference, which will be held in Naples (Italy) from April 21st to April 23rd, a half-day tutorial is organized on Friday, 24th April. This tutorial is dedicated to the trend in technology, design, test and dependability of tomorrow memories.

The Memories of Tomorrow: Technology, Design, Test, and Dependability

Abstract:

Fast, cheap, dense and dependable; that's what we look for in an embedded memory device. The memories of today, more often than not, fail to comply with at least one of these requirements, especially due to technology limitations. The challenges faced by the well-established memories in ultra-scaled technologies have brought forth the need for alternate storage devices. This tutorial provides an overview of the major obstacles faced by today technologies and opens the path towards understanding the emerging memory technologies and the challenges they pose to design and test engineers alike. The focus will be placed on magnetic RAMs as well as various resistive RAMs.

Presenter: Elena Ioana VATAJELU

Bio:

Elena Ioana Vatajelu received her MSc degree in physics engineering from Babes-Bolyai University of Cluj Napoca, Romania and her PhD degree in electronics from Universitat Politecnica de Catalunya (UPC) Barcelona, Spain. She is currently a Research Assistant in the department of Informatics and Control Engineering (DAUIN) at Politecnico di Torino, Italy. Previously, she was with LIRMM, Montpellier, France in a Post-Doctoral Research position. Her current research activity is focused on emerging memory technologies with special emphasis on spin-based devices. She is mainly focusing on the characterization of fabrication-induced process variability based on statistical data; modeling and characterization of aging-induced parameter variation; design and reliability of emerging memory systems; analysis of possible use in hardware security: Physically Unclonable Functions; secret key generation exploiting control signals settings; MRAM Security Analysis under Different Kind of Attacks. She serves as member of the Program and Organizing Committees of several IEEE events (DATE, VTS, ETS, etc).